[Total No. of Ques. 05] Seat No: [Total No. of Pages: 01]

G H Raisoni College of Engineering and Management, Pune.
(An Autonomous Institution affiliated to Savitribai Phule ,Pune University)
FY B.TECH (TERM II /SEM II)
ESE SUMMER 2024 (2020 Pattern)
Digital Logic Design (UECL103)

[Time: 02 Hours] [Max. Marks--50]

Instructions to the candidates:
1) *All questions compulsory.*
2) *Neat diagrams must be drawn wherever necessary.*
3) *Figures to the right indicate full marks.*
4) *Assume suitable data, if necessary.*
5) *Other Instructions, if any.*

Q. No.	Sub Questions	Questions	Marks	CO	BL
1	a)	a) $(83)_{10} = (?)_2$ b) $(313)_{10} = (?)_8$ c) $(122)_{10} = (?)_{10}$	[6]	CO1	L2
	b)	Implement Following SOP form using logic gates a) F1 = $\sum$m(1, 2,4,7) b) F2 = $\sum$m(0,2,6)	[4]	CO1	L2
2	a)	Explain the following Boolean Laws with suitable examples a) Commutative Law b) Associative Law c) Demorgan's Law	[6]	CO3	L1
	b)	Describe CMOS inverter circuit with the help of Truth Table	[4]	CO2	L2
3	a)	Explain 8:1 Multiplexer with the help of equation truth table and logical diagram.	[6]	CO3	L3
	b)	Design 4- bits Gray code to Binary Converter	[4]	CO2	L2
4	a)	Draw and explain 3- bit Ripple up Counter with Waveforms.	[6]	CO4	L2
	b)	What is Race around condition in JK Flip Flop? How it is eliminated.	[4]	CO4	L2
		OR			
	c)	What are different types of Registers? Draw and explain Left Shift Operation of Shift Register with Waveforms.	[4]	CO4	L2
5	a)	Draw and explain mealy machine with proper block diagrams.	[6]	CO5	L4
		OR			
	b)	Draw and explain Moore machine with proper block diagrams.	[6]	CO5	L4
	c)	Draw and explain sequence detector for the sequence ---0011--- using Mealy FSM.	[4]	CO5	L4